**Date:**

**Ahsanullah University of Science and Technology**

Department of Computer Science and Engineering

Third Year, First Semester Final Examination, Fall 2015

Course No: **CSE 3109** Course Title: **Digital System Design**

Time: 3 Hours Full Marks: 70

**[ There are 7(Seven) questions. Answer any 5(Five) questions.]**

**[*Marks allotted are indicated in the right margin within ‘[ ]’.*]**

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| --- | --- | --- |
| 1.a) | What is programmable logic array? Draw the block diagram of PLA. | [3] |
| b) | A combinational circuit is defined by the functions:  F1(A,B,C) = ∑ (3, 5, 6, 7)  F2(A,B,C) = ∑ (0, 2, 4, 7)  Implement the circuit with a PLA having three inputs, four product terms, and two outputs. | [5] |
| c) | The traffic lights on a main road show green for 50 s, yellow for 6 s, and red for 30 s. Bits 1, 2 and 3 of port 4 of SAP-2 are the control inputs to peripheral equipment that runs these traffic lights. Write a program in mnemonics for SAP-2 that produces time delays of 50, 6 and 30 s for the traffic lights. | [6] |
| 2.a) | What is Shift Register? What are the differences between RAM and ROM? | [4] |
| b) | Describe the architecture of SAP-1. | [6] |
| c) | Write a program for SAP-1 to solve this arithmetic problem.  16 + 20 + 24 – 32  The numbers are in decimal form. | [4] |
| 3.a) | Design a 4-bit binary counter. | [4] |
| b) | What is Modified Booth’s algorithm? Explain with example. | [4] |
| c) | Show all the steps of Booth’s algorithm for the following 6 bit numbers:  X= 10 Y = -16 | [6] |
| 4.a) | What is the difference between hard-wired control and microprogram control? What are the advantage and disadvantage in each method? | [4] |
| b) | **Figure 1:** control state diagram for problem 4 b)   |  | | --- | | z = 0    x = 0 x = 1 y = 1    y = 0      z = 1 | | [10] |
|  | The state diagram of a control unit is shown in Figure 1. It has eight states and three inputs x, y and z. Design the control by the sequence register and decoder method with JK flip-flops G3, G2 and G1. Use the flip-flop outputs as conditions for the present states. |  |
| 5.a) | Draw the block diagram of an 8-bit ALU with a 4-bit status register. The four status bits are symbolized by C, S, Z and V. | [3] |
| b) | Prove that the multiplication of two **n-digit** numbers in any base **r** gives a product of no more than **2n** digits in length. | [4] |
| c) | Deign an arithmetic circuit with two selection variables S1 and S0, that generates the following arithmetic operations. Draw the logic diagram of one typical stage.   |  |  |  |  | | --- | --- | --- | --- | | S1 | S0 | Cin = 0 | Cin = 1 | | 0 | 0 | F = A + B | F = A + B + 1 | | 0 | 1 | F = A | F = A + 1 | | 1 | 0 | F = B’ | F = B’ + 1 | | 1 | 1 | F = A + B’ | F = A + B’ +1 | | [7] |
| 6.a) | The following register-transfer operations specify a four-state control of the sequence register and decoder type. G is a 2-bit sequence register and T0, T1, T2 and T3 are the outputs of the decoder.  xT0: G G+1  yT0: G 10  zT0: G 11  T1+T2+T3: G G+1  Draw the state diagram of the control and design the sequence register with JK flip-flops. | [7] |
| b) | The symbolic microprogram for control memory is given below:   |  |  |  | | --- | --- | --- | | ROM  address | Microinstruction | Comments | | 0 | x = 1,if (qs = 1) then ( go to 1), if (qa = 1) then ( go to 2), if ( qs ^ qa = 0) then ( go to 0) | Load 0 or external addres | | 1 | Bs ⃪ Bs’ | qs = 1, start subtraction | | 2 | If ( S = 1) then ( go to 4) | qa = 1, start addition | | 3 | A ⃪ A + B, E ⃪ Cout , go to 0 | Add magnitudes and return | | 4 | A ⃪ A + B’ + 1, E ⃪ Cout | Subtract magnitudes | | 5 | If ( E = 1) then ( go to 0), E ⃪ 0 | Operation terminated if E = 1 | | 6 | A ⃪ A’ | E = 0, complement A | | 7 | A ⃪ A + 1, As ⃪ As’, go to 0 | Done, return to address 0 |   Here L variable loads A and E from ALU, y variable complements Bs , z variable complements As and w variable clears E. And the ALU has the following function table:   |  |  |  |  |  | | --- | --- | --- | --- | --- | | S2 | S1 | S0 | Cin | Output | | 0 | 0 | 1 | 0 | F = A + B | | 0 | 1 | 0 | 1 | F = A - B | | 1 | 1 | 1 | 0 | F = A’ | | 0 | 0 | 0 | 1 | F = A + 1 |   Write the binary microprogram for the control memory and also draw microprogram control block diagram. | [7] |
| 7.a) | Draw the block diagram and logic diagram of a RAM. | [2] |
| b) | Design an arithmetic circuit with one selection variable s and two data inputs A and B. When s = 0, the circuit performs the addition operation F = A + B. When s = 1, the circuit performs the decrement operation F = A - 1. | [3] |
| c) | Draw the LDA and SUB routines of SAP-1 and also their fetch and execution timing diagram. | [4] |
| d) | The inputs to each full-adder circuit of an arithmetic logic unit are according to the following Boolean functions:  Xi = AiBi + (s2s1’s0’)’Ai + s2s1s0’Bi  Yi = s0Bi + s1Bi’(s2s1s0’)’  Zi = s2’Ci  Determine the 12 functions of the ALU. | [5] |